10GHz PLL local oscillator (Solilock10G version 2), JF1WKX, Nobuo Katsuma

Introduction

I have presented a PLL oscillator that consists of a 4-to-6GHz direct oscillator and a doubler. For higher-frequency transverters, I developed a new PLL oscillator, Solilock10G version 2, with improved phase noise and wider frequency coverage of up to 17 GHz.

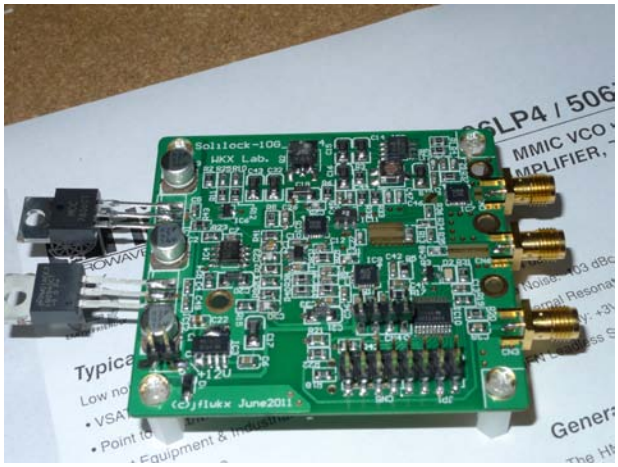


Photo 1 Entire circuit placed on a board, including RF circuitry (oscillator, multiplier, and PLL), controller, power supply, and PLL loop filter

1. RF circuit

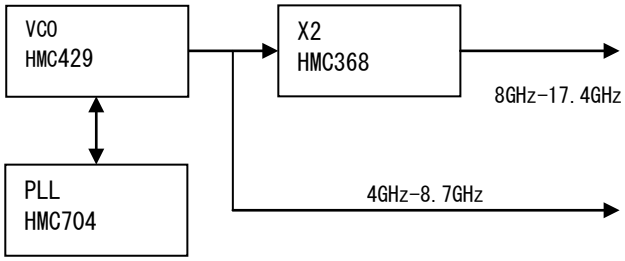


Fig.1 Block diagram of Solilock10G ver.2

I used three Hittite's ICs of VCO (HMC429), doubler (HMC368), and PLL (HMC704), as shown in Fig. 1. The output of VCO is amplified and its frequency is doubled. Small portion of the output is fed into the PLL IC. We can set a dividing factor of HMC704 with the accuracy of 19-bit integer and 24-bit fraction, An HMC704's diagram is shown in Fig. 2. When a reference signal of 100 MHz is used, a frequency step of 5.96 Hz is achieved near 10 GHz.

HMC704's phase noise becomes smaller than that of HMC700 that was employed in my previous work (Solilock10G ver. 1). The phase noise spectra of the version 1 and 2 are shown in Fig. 3. The phase noise of HMC704 is estimated to be -115 dBc/Hz at 5 GHz, which may satisfy my goal of -100 dBc/Hz at 10 GHz.

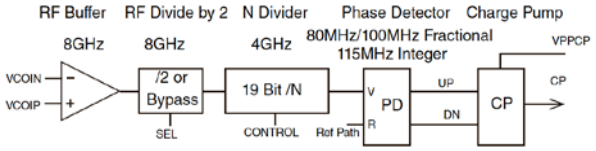


Fig.2 RF path of HMC704 (from data sheet)

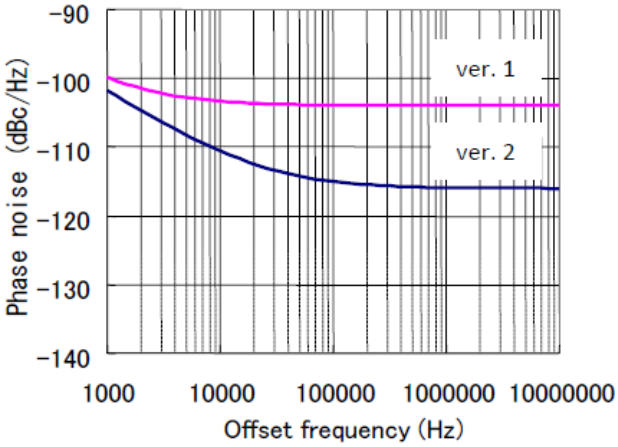


Fig. 3 Phase noise spectra of Solilock10G's

2. Controller

A TI's 16-bit microcomputer MSP430F2121 is used to control PLL IC. We can stop CLOCK in the CPU and wake it up via serial interface, which means the spur emission could be the lowest in operation and the CPU is readily open for commands. The developer kit, IAR Kickstart (4kB version), supports 64-bit operation. Thanks to this precision, even 1 Hz can be expressed in integer at 10 GHz. A 1mHz setting is actually possible.

3. Power unit

3-1) VCO power supply

A high-performance PLL needs a low-noise power supply (PS). The PS specifications have

to be determined so as to achieve the phase noise estimate (-115 dBc/Hz).

As the VCO voltage changes due to noise or drift, an oscillation frequency is changed as well, which is called pushing. If the noise frequency is within the PLL's loop frequency, the noise is reduced due to negative feedback. Otherwise, the noise outside the loop frequency is output unfortunately. We read in a data sheet of HMC506 or Fig. 4 that the phase noise of -115 dBc/Hz can be obtained at 200kHz offset frequency. The pushing of HMC506 is 78 MHz/V. To achieve the phase noise of -125 dBc/Hz at 200kHz offset with the VCO such as HMC506, the PS noise must be smaller than 2.0 nV/Hz$^{1/2}$. Note that a conventional three-terminal regulator such as 78 series emits approximately 200 nV/Hz$^{1/2}$ so that these cannot be used in this kind of circuit. Even low-noise regulators output noise level of 20 nV/Hz. The last candidate might be a Hittite's 3 nV/Hz$^{1/2}$ PS IC (HMC860LP3E) although I have not tested it experimentally.

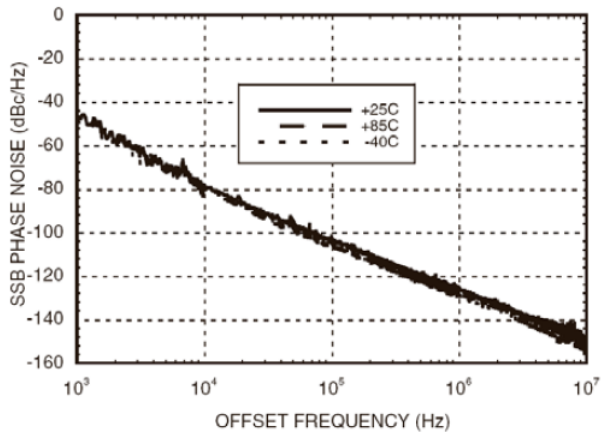


Fig.4 Phase noise of HMC506 (from data sheet)

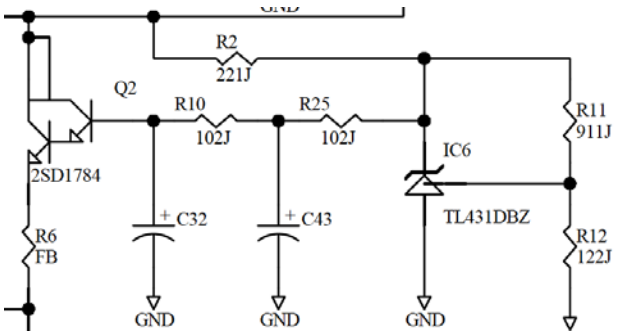


Fig.5 VCO power supply

A VCO PS circuit is shown in Fig. 5. A reference voltage is generated in TL431 and, then, amplified by Darlington transistors. Two-stage CR filters (1kΩ, 10μF) are connected to the base. The phase noise measurement results are shown in Fig. 6. It is understood that the PS performance strongly affect the phase noise. The Fig. 5 circuit was employed in this work.

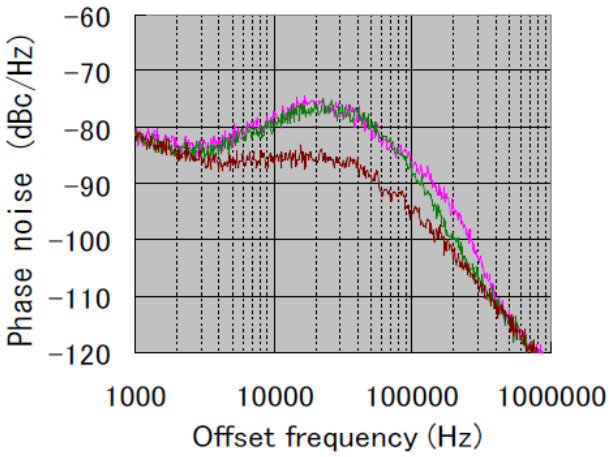


Fig.6 Phase noise spectra. From high to low noise, 78 series (78M33), LDO for VCO (TPS79633), and very low noise one (Fig. 5).

3-2) PLL IC power supply

A TI's LP2985-50 is employed for a phase comparator (5 V) and TPS79633 for the rest of the circuit (3.3 V).

4. Loop filter

4-1) Loop gain of PLL

A loop filter is inserted between the PLL IC's charge pump output and the VCO's control terminal. While the charge pump outputs CURRENT (i_0), the VCO's control terminal accepts VOLTAGE (v_2). The loop filter consists of a pre-filter (R1, C1), an active filter (R2, C2, C3) and a post-filter (R3, C4).

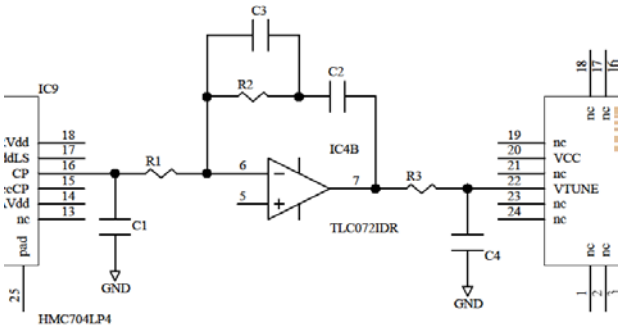


Fig. 7 Loop filter

The relationship between i_0 and i_1 (a current from the pre-filter to a negative input) is as follows:

$$i_1 = \frac{1}{1+ j\omega C_1 R_1} \times i_0$$

At the active filter with R2, C2, and C3, i_1 is converted into v2;

$$v_2 = \frac{1}{j\omega C_2}\left(\frac{1+ j\omega(C_2 + C_3)R_2}{1+ j\omega C_3 R_2}\right) \times i_1$$

The VCO control voltage, v_3, is expressed, using R3 and C4 in the post filter;

$$v_3 = \frac{1}{1+ j\omega C_4 R_3} \times v_2$$

A gain of a frequency divider K_{DIV} is

$$K_{DIV} = \frac{f_{PFD}}{f_{VCO}} = \frac{1}{N},$$

where f_{PFD} is a frequency of the phase frequency detector and f_{VCO} is an oscillation frequency of PLL. A gain of the phase detector K_{PD} is

$$K_{PD} = \frac{I_{CP}}{2\pi}$$

We can set I_{CP} by a register of the PLL IC. Finally, a gain of the VCO, K_{VCO} becomes

$$K_{VCO} = \frac{\Delta f_{VCO}}{\Delta v}$$

We can measure this value experimentally or employ the value in the data sheet. As a result, a transfer function of the PLL loop becomes

$$P(s) = \frac{K_{DIV} K_{PFD} K_{VCO} Z(s)}{s}$$

where Z(s) is a loop filter's transfer function. Since a frequency is converted to a phase, the equation has a s^{-1} part. K_{PD}, K_{VCO}, and K_{DIV} are determined by circuit requirements, and then we have to tune the PLL by the adjustments of R1, R2, C1, C2, C3, and C4.

The following are procedures of fixation of loop filter's constant.

i) Determine a loop frequency range and phase margin.

ii) Calculate C1 and R1, assuming that the cutoff frequency of the pre-filter as about 30 times the loop range.

iii) Calculate R3 and C4, assuming the cutoff frequency of the post filter as about 10 times the loop range.

iv) Calculate R2, C2, and C3, being based on the phase margin and frequency range. The details are in Refs. 1-2).

v) Do the final adjustments of R2, C2, and C3, measuring the off-range noise experimentally. This process is not always necessary.

We had to carry out these procedures using Excel or a similar tool but now the calculation becomes quite easier by using calculation applications provided by IC manufacturers. ADIsimPLL by Analog Devices was used for this design.

4-2) Filter constant

ADIsimPLL is prepared for Analog Devices' IC of course. It needs some ideas to apply it to other manufactures' IC. As for ADF4156 that is supported in ADIsimPLL (ver. 3.4), the maxima of f_{VCO} and f_{PFD} are 6.2 GHz and 26 MHz, respectively. Then, we have to covert some parameters to put them into the ranges above.

Here is an example. The f_{PFD} of HMC704 is 50MHz. What should we do? Look at the transfer function. It is separated into a gain and a frequency section. The gain part

$K_{DIV}K_{PFD}K_{VCO}$ does not care which one is large or small. It cares only the product. If K_{PFD} becomes 1/2, then let us make K_{VCO} twice.

An example:

Oscillate the VCO (HMC506) at 8.4 GHz, where K_{VCO} is 20 MHz/V. Operate it at f_{PFD} of 50 MHz.

Input 4.2 GHz (=8.4/2) to a VCO input counter of ADF4156. Input 10 MHz (=50/5) to f_{PFD}. Since we input different values to f_{VCO} and f_{PFD} we have to adjust the loop gain by K_{VCO}. Actual K_{VCO} is 120 MHz/V but we have to modify it to 300 MHz (=(50/10)x(42/84)x120). Now we can calculate constants by using ADIsimPLL. It is confirmed values are really correct.

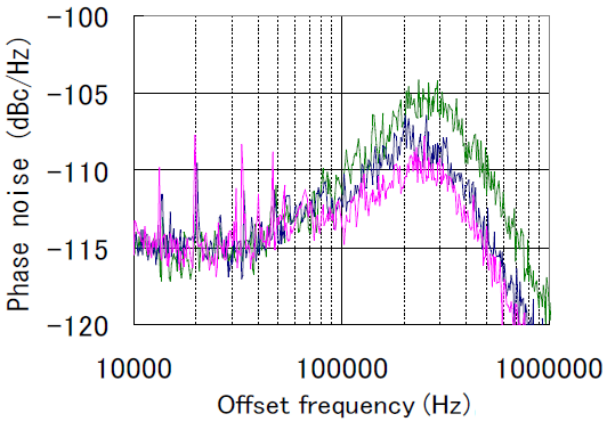
4-3) Selection of op-amplifier

The noise from amplifier is the key issue. Note K_{VCO} is 120 MHz/V. The VCO phase noise (-115 dBc/Hz at 200kHz offset) is equivalent to a noise of 4.2 nV/Hz$^{1/2}$ at the input terminal of voltage control. We have to choose the op amplifiers with the noise sufficiently lower than 4.2 nV/Hz$^{1/2}$. Table 1 summarizes noise level of three kinds of op amplifiers. LTC6201 may be good but TLC072 outputs 5.6dB-larger noise.

I measured noise spectra of these amplifiers, as shown in Fig. 8. The results agree to the prediction in Table 1. The noise of TLC072 is about 5 dB larger than that of LT6201.

Table 1 Noise comparison among op amplifiers (unit: nV/Hz$^{1/2}$)

	Input equivalent noise	Sum of the left and 4.2nV/Hz$^{1/2}$
TLC072	7	8.2
AD8028	4.3	6
LT6201	0.95	4.3



Fig, 8 Phase noise degradation by op amplifiers. From high to low noise, TLC072, AD8028, and LT6201.

5. Reference oscillator

A reference oscillator is quite important for this kind of millimeter-wave application. The phase noise from a 100MHz oscillator is increased 34 dB at 5 GHz. We need the phase noise specification of -150 dBc/Hz at OCXO output. Fig. 9 shows phase noise spectra of my junk OCXO. From the results, the phase noise -150 or -155 dBc/Hz may be obtained.

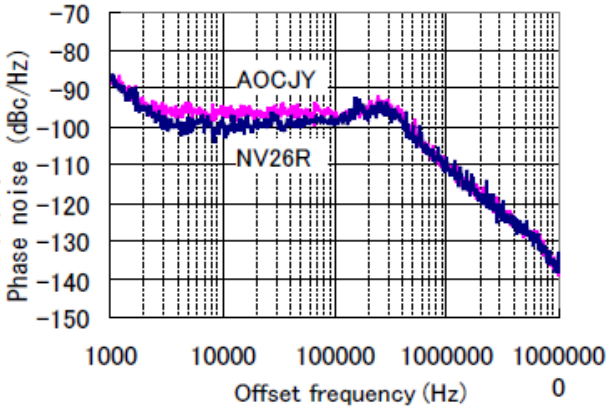


Fig.9 Phase noise spectra of two types of my junk OCXO. Measured at 11.37GHz.

6. Results

After design and manufacturing, I built the entire circuit in an appendix figure. The obtained phase noise was -115 dBc/Hz at 4.5 GHz at the integer mode and was -100 dBc/Hz at 11.37 GHz at the fractional mode. These results are shown in Figs. 10 and 11.

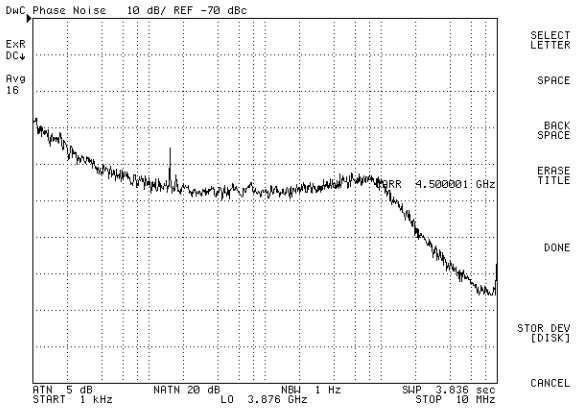


Fig.10 Phase noise at 4.5GHz

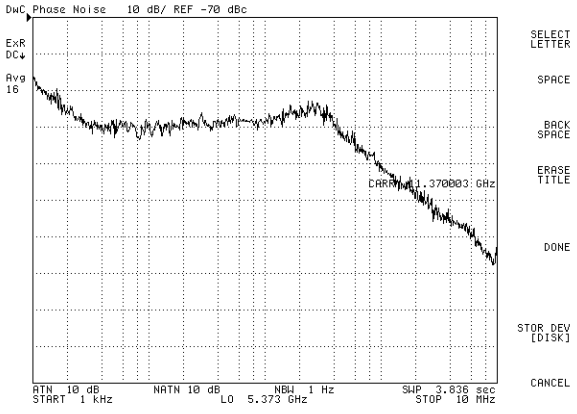


Fig.11 Phase noise at 11.37GHz.

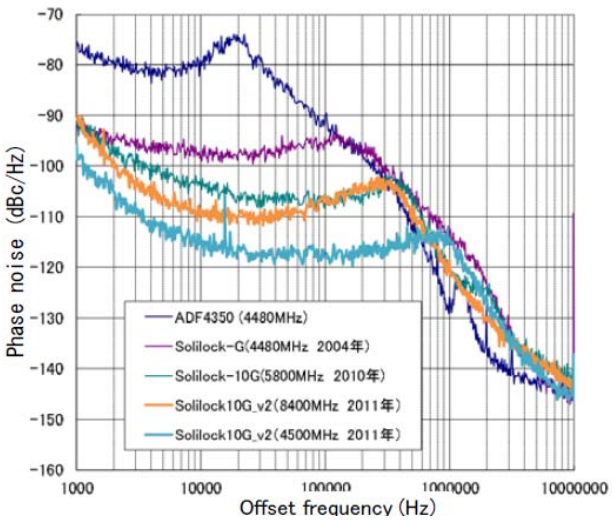


Fig.12 Phase noise comparison among the ICs

Figure 12 summarizes phase noises of the Solilock's. As for ADF4350, the measurement was done by using a commercial PLL board. Among the four Solilock versions, the newest one, Solilock10G ver. 2 (HMC704), exhibits the lowest phase noise. In case of 10MHz reference signal usage, we cannot obtain the phase noise better than -100 dBc/Hz at 5.8 GHz. If the better characteristic is needed, a higher frequency reference such as 100 MHz seems required.

Since the Solilock's directly oscillates GHz bands, spurious emission is free, as shown in Fig. 13.

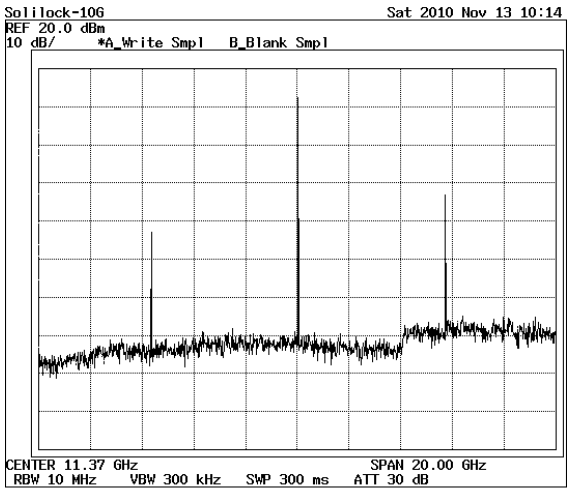


Fig.13 Spectrum near 11.37GHz (+/-10GHz)

7. Conclusion

I designed and developed a new version of PLL oscillator, Solilock10G version 2. It can be built by using only commercial devices. Solilock oscillates microwave frequencies directly with low phase noise. As my final summary, I compared the Solilick10G ver. 2 (8.4 GHz) with a different type of oscillator, a VHF VCXO PLL. As shown in Fig. 14, the phase noises within the band are almost the same but, at the 100k to 2MHz range, the VHF VCXO PLL exhibits the better phase noise.

Experimental data in the website of Luis, CT1DMK, are gratefully appreciated.

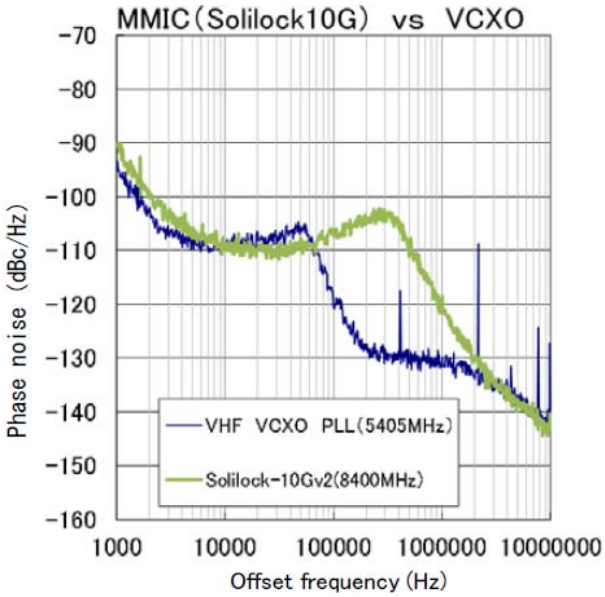


Fig.14 Phase noise comparison between Solilock (higher) and VCXO (lower)

References

(1) Dean Banerjee, 'PLL Performance Simulation and Design Handbook 4th Edition', PDF available onlin.

(2) N. Katsuma, JF1WKX, 'Design of PLL loop filter', HAM Journal No. 91 (1994), pp.98-109, in Japanese.

(3) Hittite: data sheets.

(4) http://www.qsl.net/ct1dmk/reflock.html